UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,431	01/17/2002	Chris Yoochang Chung	UNIV0123	3518

7590 09/22/2005

Ronald M. Anderson
LAW OFFICES OF RONALD M. ANDERSON
Suite 507
600 - 108th Avenue N.E.
Bellevue, WA 98004

EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,431	CHUNG ET AL.	
	Examiner	Art Unit	
	Hau H. Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-30* is/are pending in the application.

4a) Of the above claim(s) *2* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *17-30* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Status of Claims

1. Restriction requirement: The examiner acknowledges Applicant's election filed on June 10, 2004 to elect group I (claims 1, 3-16). Since the petition requesting the Director reviewing the restriction is denied, claims 17-30 (groups II to IV) are withdrawn from consideration.

Response to Arguments

2. Applicant's arguments filed June 24, 2005 have been fully considered but they are not persuasive.

In response to Applicant's argument that the cited references do not disclose all the claimed features, the examiner disagrees. In particular, with regard to Applicant's arguments that reference Ezer et al. does not teach the claimed 'enhanced texture cache', the examiner has pointed out in the previous Office Action, that Ezer et al. teach a texture memory buffer 425 that "is used for 3-D graphics as well as motion compensation pertaining to MPEG. Thus, the texture memory 425 is shared between texture mapping and MPEG video processing" (col. 8, lines 33-36). Therefore, texture memory buffer 425 is not limited to storage of one type of multimedia data. Further, with reference to Fig. 4, Ezer et al. teaches the texture memory buffers 425 located in the display processor 203, not in common memory 103 as asserted by Applicant. Since Van Hook et al. teach a display processor 500 performing programmable graphics pipeline processing multimedia, having a texture memory 502 and also teach an instruction cache, register file, and vector functional unit, Ezer et al. also teach a display processor 203 performing 3D graphics pipeline and video processing having a texture memory that can store more than one type of multimedia data, it would have been obvious to one skilled in the art to utilize the method as

taught by Ezer et al. in combination with the method as taught by Van Hook et al. in order to avoid the need for a duplicate memory system (col. 4, lines 64-67, and col. 5, lines 1-2) (thereby reducing the need for another memory for video processing).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook et al. (U.S. Patent No. 6,342,892) in view of Ezer et al. (U.S. Patent No. 6,275,239).

Referring to claims 1 and 16, Van Hook et al. teach a graphics pipeline comprising a signal processor 400 as shown in Fig. 6. As shown in Fig. 7, the signal processor 400 includes an instruction memory 402 (instruction cache) for storing microcode for execution by vector unit 420, a plurality of register files 422 (0)-422(7), a vector processing unit 420, which comprises eight 16-bit calculating elements capable of performing numerical calculations in parallel (thus, includes a plurality of vector functional units). Vector unit 420 is especially suited for graphics matrix calculations and certain kinds of digital audio signal processing operations (performing graphics and media instructions) (col.15, lines 60-67, and col. 16, lines 1-11). Van Hook et al. also teach a texture memory 502 as shown in Fig. 6.

Thus, van Hook et al. teach all the limitations of claim 1 except that the vector unit obtains from the texture cache a vector of at least one partition of the multimedia.

However, Ezer et al. teach an integrated media coprocessor chip which partitions 3-D graphics, video, and audio tasks through time division multiplexing (col. 2, lines 10-12), wherein as shown in Fig. 4, comprising a texture memory buffers 425 of the display processor 203 all source image data used for texturing and is shared between texture mapping and MPEG video processing (col. 8, lines 16-36). Ezer et al. further teach the media digital signal processor (MSP) 804 is programmed to perform the signal processing portion of video and audio compression/decompression (media processing) and to perform fixed point geometry processing for 3-D graphics (graphics processing). The integer vector computation of the MSP has enough precision for limited precision for 3-D graphics applications (e.g., a 10-bit image coordinate range, 8-bit colors, and 16-bit depth values) (col. 10, lines 41-65). An applications data flow diagram is shown in Fig. 9.

Since Van Hook et al. teach a vector functional unit that can perform graphics and media operations, and Ezer et al. teach a texture cache that can store multimedia data, it would have been obvious to one skilled in the art to utilize the method as taught by Ezer et al. in combination with the method as taught by Van Hook et al. in order to avoid the need for a duplicate memory system (col. 4, lines 64-67, and col. 5, lines 1-2).

In regard to claim 10, as shown in Fig. 6, Van Hook et al. teach the color combiner 508 combines and interpolates between the texture color and a color associated with the graphic primitive. Blender 510 blends the resulting pixels with pixels in frame buffer 118, and is also

involved in performing Z buffering (i.e., for hidden surface removal and anti-aliasing operations) (col. 16, lines 16-31).

Referring to claims 11 and 12, Van Hook et al. shows in FIG. 7A an example of a register instruction format 450 and how signal processor 400 uses that register instruction format to access three 128-bit wide words 452 within data memory 404. Register instruction format 450 may include a 6-bit operation code field 450(a), a 5-bit source register specifier 450(b), a 5-bit target (source/destination) register specifier 450(c), a 5-bit destination register specifier 450(d), and a parameter field 450(e). As shown in FIG. 7B, Van Hook et al. teach vector unit 420 treats each of these 128-bit words as a concatenated sequence of eight 16-bit values (output buffer), and operates on each of the 16-bit values in parallel (col. 18, lines 37-54) (partitioned data).

In regard to claims 13 and 14, as shown in Fig. 6, Van Hook et al. teach a memory interface 512 (write buffer) coupled to a blender 510 for performing read, modify and write operations for the individual pixels, and also has special modes for loading/copying texture memory 502, filling rectangles (fast clears), and copying multiple pixels from the texture memory 502 into the frame buffer 118. Memory interface 512 has one or more pixel caches to reduce the number of accesses to main memory 300 (col. 16, lines 31-37).

In regard to claims 15, although Van Hook et al. does not teach a configuration register for providing the vector unit with partitioned data access, thereby instructing the vector unit to perform one of graphics process and media process, Ezer et al., as shown in Fig. 5, teach a time frame 501 is partitioned into three parts. The first partition 502 is used to perform video functions; the second partition 503 is used to perform audio functions; and the third partition 504

is used to perform 3-D graphics functions. The times for performing each of the video, audio, and 3-D graphics functions are variable.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Ezer et al. in combination with the method as taught by Van Hook et al. in order to correctly perform functions depending on the assigned data types.

5. Claims 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook et al. (U.S. Patent No. 6,342,892) in view of Ezer et al. (U.S. Patent No. 6,275,239) and further in view of Gossett (U.S. Patent No. 6,104,415).

Referring to claim 3, as cited above, Van Hook et al. and Ezer et al. teach all the limitations of claim 3, except that the texture cache includes a line buffer and cache areas, the graphics pipeline further includes a texture address unit in communication with the texture cache.

However, Gossett teaches a graphics pipeline comprising a texture cache 74 coupled to a texture address unit 68 as shown in Fig. 5. As shown in FIG. 10, texture cache 74 comprises table 75 and memory 87. Memory 87 stores the data associated with the texture cache 74 (texture cache area) (col. 16, lines 16-21). Gossett further teach the textures originate from the SDRAM 50, and are loaded along the 256-bit bus 77 into the format unit 76, which expands or compresses the formats depending upon in what format the texture was stored. Then, a portion of that texture image is loaded into the texture cache 74 (a line buffer providing multiple read ports for accessing texture cache area) (col. 12, lines 13-17).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Gossett in combination with the method as taught by Van Hook et al. and Ezer et al. in

order to accelerate minified texture cache access of the computer graphics hardware (col. 1, lines 26-30).

In regard to claims 4 and 5, with reference to Fig. 23, Van Hook et al. teach texture coordinate unit 530 (texture address unit) computes appropriate texture coordinates for mapping texture stored within texture memory 502 onto the primitive being rendered (col. 50, lines 34-41). Van Hook et al. further teach texture coordinate unit 530 then generates an offset into texture memory 502 based on these tile coordinates. The texture coordinate unit 530 in this example can address 2 x 2 regions of texels in one or two cycle mode, or 4 x 1 regions in copy mode (arbitrary-sized block). Texture coordinate unit 530 also generates S/T/L fraction values (filter coefficients) that are used to bi-linearly or tri-linearly interpolate the texels (col. 51, lines 51-57).

Referring to claims 6 and 7, as shown in Fig. 18, Van Hook et al. teach the first operation display processor 500 performs on an incoming primitive (which can be lines, triangles, rectangles, col. 45, lines 4-7) is to rasterize the primitive, i.e., to generate pixels that cover the interior of the primitive (FIG. 18, block 550). Rasterize block 550 (rasterization unit) generates various attributes (e.g., screen location, depth, RGBA color information, texture coordinates and other parameters, and a coverage value) for each pixel within the primitive. Rasterize block 550 outputs the texture coordinates and parameters to a texture block 552. Texture block 552 accesses texture information stored within texture memory 502, and applies ("maps") a texel (texture element) of a specified texture within the texture memory onto each pixel outputted by rasterized block 550 (col. 45, lines 10-24).

In regard to claims 8 and 9, as also shown in Fig. 18, Van Hook et al. teach a z-buffer operation 564 (in communication with the rasterization unit 550) performs hidden surface removal (i.e., so closer opaque objects obscure objects further away), and cause the new pixel value to be written back into frame buffer 118 (col. 45, lines 35-40).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 571-272-7778.

The fax number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-2 17-9197 (toll-free).

H. Nguyen

09/16/2005

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600